**Chapter 2: 8085 PINS**

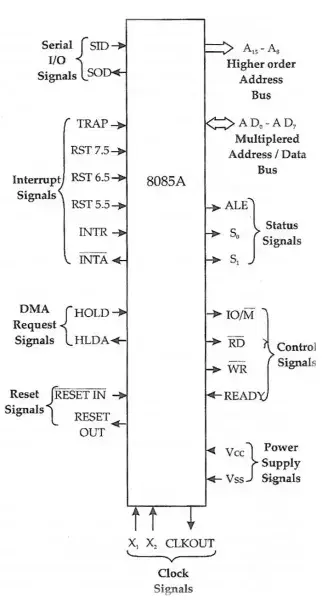
**Topic – 1: Intel 8085**

**Must Know Information**

* **8-bit** microprocessor (**8-bit** long ***data bus***).
* Means it can handle **8-bit** long data.
* This data can move **bidirectionally**.
* Means from **accumulator** to **memory register** & vice versa.

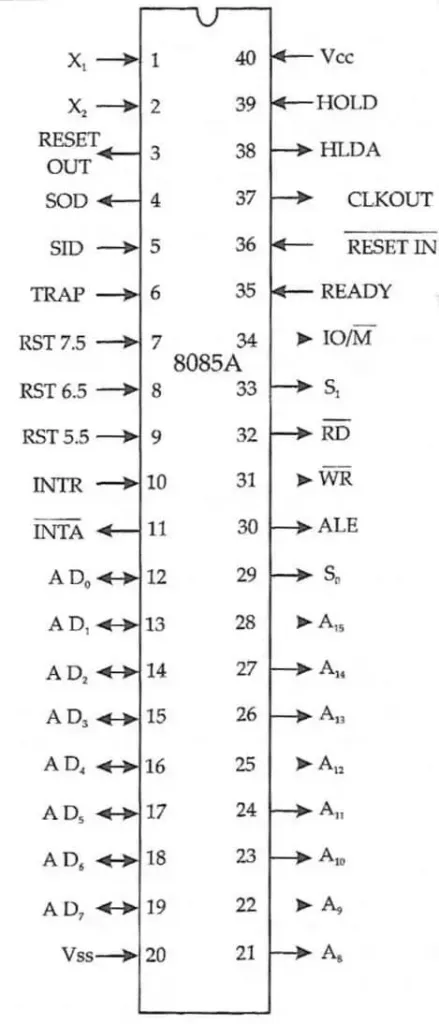
**Topic – 2: Pin Diagram**

**Nine Groups of Pins**



* We call this diagram as ***logic pinout***.
* These pins in it are classified into **nine groups**, on the basis of **signals** they produce.

**Ungrouped Pin Diagram Along With Pin Numbers**



**Topic – 3: Pin Description**

**Lower-Order Address Bits**

* **AD0 – AD7**
* Also known as ***data bus***.
* These pins are connected to **I/O devices** & **memory**.
* These pins use **multiplexed circuits** & are **demultiplexed** back using **ALE** pin.
* In the **first machine cycle**, these address buses are **accessed** & their **bits** are **set**.
* And in **second machine cycle**, their **bit** values are **copied** to latches called **74LS373 IC**.
* So, we get total of **16-bit** data **=** **8-bits** at **address lines** **+** **8-bits** at **latches**.

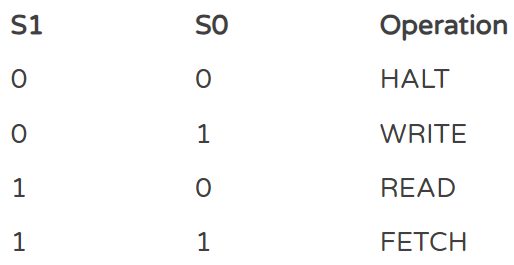
**Higher-Order Address Bits**

* **A8 – A15**
* The addressing capability of **higher-order address bus** is **more** than **lower-order**.
* So, the **higher-order address bus** access those locations where lower-order bits **can’t** reach.

***\*Multiplexed circuits are often result of manufacturer adding features to microprocessor without disturbing the pin configuration\****

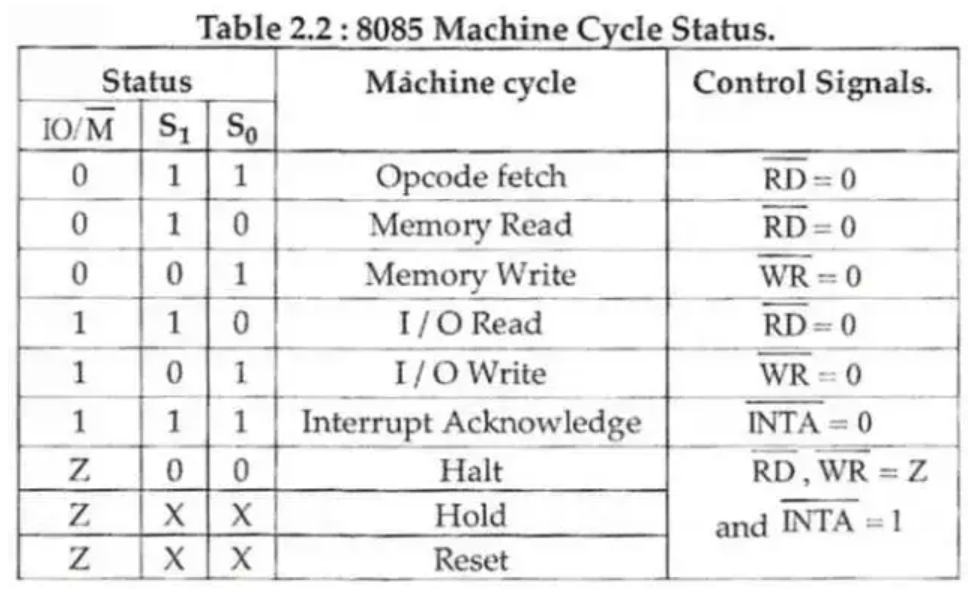
**Status Signals**

* **ALE, S0, S1**
* **ALE:** Address enable latch.
* As discussed earlier, **ALE** sends **positive pulse** to activate **external IC latches** during **first machine cycle**.
* **S1 and S0:** Status signals.
* These tell what kind of operation is being performed by the microprocessor through its **bit patterns**.



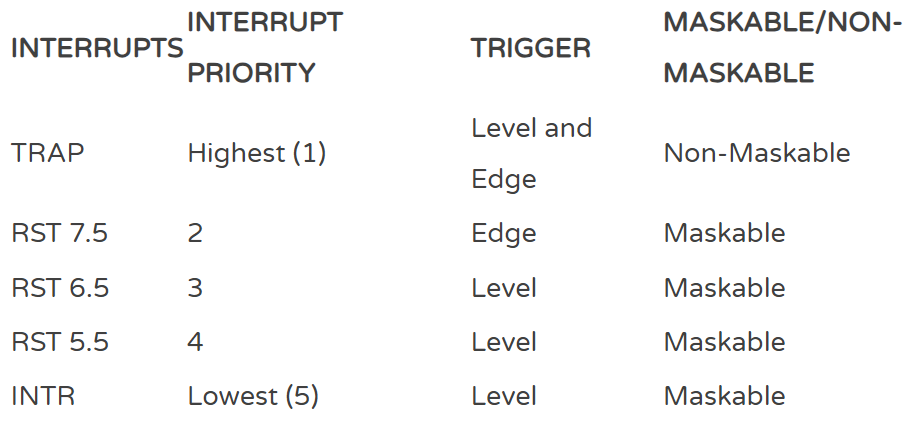
**Control Signals**

* **RD, WR and IO/M**
* **RD:** Used for **reading** & is an **active low pin**.
* Means when it is set to **0**, it **reads** data from the **memory** or **I/O**.
* And pastes them to the **lower-order address bits**.
* **WR:** Another active low pin used for **writing**.
* When it is set to **0**, it pastes the data in **lower-order address bits** to **memory** or **I/O**.
* **IO/M:** Input output/ memory.
* Just a **status signal pin** like **S0** and **S1** & thus, used along with them.
* It helps determining which **machine cycle** is being processed & if currently **memory** or **I/O** is involved in data transfer.



**Interrupt Signals**

* **TRAP, RST 7.5, RST 6.5, RST 5.5, INTR, INTA**
* Also known as **maskable vector interrupts**.
* Emits signal to **interrupt** normal flow of program.
* Whenever the interrupt receives signal, certain programs **start executing** as per which interrupt is activated (in order of preference).
* But these can be **masked** (disabled) **using code**.
* **INTR:** Interrupt request, **lowest priority interrupt** which is executed after the running program ends.
* After the signal from **INTR** gets acknowledged by microprocessor, **INTA** is activated.
* **INTA:** Interrupt acknowledgement.



**Clock Signals**

* **X1, X2, CLKOUT**
* Pin **X1** and **X2** are used for connecting **external crystal oscillator** to them.
* **Crystal oscillator:** Used for generating **clock signals** & made up from **quartz**.
* **Intel** introduced **internal** crystal oscillator from **8085** itself.
* **Crystal oscillator** is often called as **clock generator**.
* They however require power from **external circuits** & uses **half** the supplied power.
* It uses **half** the supplied power in order to get **pure** & **filtered** signals.
* The **power** is supplied to both **X1** and **X2** simultaneously.
* **CLKOUT** pin is used to **sync** microprocessor with other connected **peripherals**.
* Works on the **same** level of frequency that is generated by **clock generator**.

**Reset Signals**

* **RESET IN, RESET OUT**
* The **bar** on top of a pin name means that the pin is **active low**.
* **RESET IN** is an active low pin.
* It is used to **reset** the microprocessor.
* **PC** (program counter) which **keeps** **increasing** from **0** as the program is under execution, is set back to **0**.
* The microprocessor starts **reading** from the starting of the **memory address** (**0000H**).
* However, the state of **flags** & **registers** is unpredictable.
* **RESET OUT** is again an active low pin.
* Its just a **signal** used for **detecting** if microprocessor is being reset.
* And it can also **reset peripherals** connected to the microprocessor.

**DMA Signals**

* **HOLD, HLDA**
* **DMA** stands for **"Direct Memory Access"**.
* If an external device wants to use the **address bus**, then it sends **request signals** to microprocessor using **HOLD** pin.
* Then microprocessor completes its **machine cycle** & sends **acknowledgement** to that device through **HLDA** pin before handing over the control to it.
* When the bus is under control of external device, the **HLDA** pin goes **high**.

**Serial I/O Signals**

* **SID, SOD**
* **SID:** Serial input data, receives **input** for **7th bit** of the **accumulator** when a **RIM** instruction is executed.
* **SOD:** Serial output data, **outputs** the **7th bit** of the **accumulator** when a **SIM** instruction is executed.

***\*Will later see what RIM and SIM instructions are\****

**Power Supply Signals**

* **VCC:** **5V** power supply
* **VSS:** Ground